AMENDMENTS TO THE CLAIMS

The claims in this listing will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A cache memory system, comprising:

a condition generation information holder that holds information that generates a new condition, the information that generates the new condition being obtained from a processor ~~generation unit operable to generate a condition concerning a state of a processor~~;

a command holder that holds a manipulation command given by the processor;

a condition holder that holds a condition relating to a state of the processor;

a judger that judges, using the condition held by said condition holder, ~~judgment unit operable to judge~~ whether ~~or not~~ a current state of the processor satisfies the condition;

an address generator that generates ~~generation unit operable to generate~~ an address to be manipulated; ~~and~~

a manipulator that manipulates ~~manipulation unit operable to manipulate~~ a cache according to the manipulation command held by said command holder using the address generated by said address generator ~~generation unit~~, when said judger ~~judgment unit~~ judges that the condition is satisfied[[,]]; and

a condition generator that generates a new condition using one of the current state of the processor and the condition held by said condition holder, and the information that generates the new condition held by said condition generation information holder

~~wherein said condition generation unit is operable to generate a new condition in the case where said judgment unit judges that the condition is satisfied~~.

2. (Cancelled)

3. (Currently Amended) The cache memory system according to Claim 1,

wherein said condition generator generates ~~generation unit operable to generate~~ a condition concerning a value of a specific register, within the processor.

4. (Currently Amended) The cache memory system according to Claim 3,

wherein the specific register comprises ~~is~~ a program counter.

5. (Currently Amended) The cache memory system according to Claim 1,

wherein said condition generator generates ~~generation unit operable to generate~~, as the condition, one of a memory access within a specific address range and a memory access outside of the specific address range.

6. (Currently Amended) The cache memory system according to Claim 1,

wherein said condition generator generates ~~generation unit operable to generate~~, as the condition, execution of a specified ~~specific~~ instruction by the processor.

7. (Currently Amended) The cache memory system according to Claim 1,

wherein said condition generator generates ~~generation unit operable to generate~~ the new condition by performing a specified ~~specific~~ calculation on a current condition.

8. (Currently Amended) The cache memory system according to Claim 7,

wherein said condition generator generates ~~generation unit operable to: generate~~ a memory access address as the condition; and

wherein said condition generator generates ~~generate~~ the new condition by adding a constant to the current condition in [[the]] a case where said judger ~~judgment unit~~ judges that the condition is satisfied.

9. (Currently Amended) The cache memory system according to Claim 8,

wherein the constant is one of: an increment value or a decrement value in a post-increment load/store instruction executed by the processor; and

a difference value of addresses in two load/store instructions executed by the processor.

10. (Currently Amended) The cache memory system according to Claim 1,

wherein said condition generator generates ~~generation unit is operable to generate~~ plural conditions, and

wherein said judger judges ~~judgment unit is operable to judge~~ whether ~~or not~~ all of the plural conditions are satisfied.

11. (Currently Amended) The cache memory system according to Claim 1,

wherein said condition generator generates ~~generation unit is operable to generate~~ plural conditions, and

wherein said judger judges ~~judgment unit is operable to judge~~ whether ~~or not~~ any of the plural conditions are satisfied.

12. (Currently Amended) The cache memory system according to Claim 1,

wherein said manipulator ~~manipulation unit~~ includes:

a data judger that judges ~~judgment unit operable~~, in [[the]] a case where said judger ~~judgment unit~~ judges that the condition is satisfied, ~~to judge~~ whether ~~or not~~ data corresponding to the address generated by said address generator ~~generation unit~~ is stored in the cache;

a selector that selects ~~selection unit operable to select~~ a line within the cache ~~memory~~ in [[the]] a case where it is judged that the data is not stored;

an updater that performs ~~a write back unit operable to perform~~ a write back from the selected line when the selected line is valid and dirty;

a transferer that transfers ~~a transfer unit operable to transfer,~~ from a memory to the selected line after the write back, the data corresponding to the address; and

a registerer that registers ~~registration unit operable to register~~ the address as a tag, to the selected line.

13. (Currently Amended) The cache memory system according to Claim 1,

wherein said manipulator ~~manipulation unit~~ includes:

a data judger that judges ~~judgment unit operable~~, in [[the]] a case where said judger ~~judgment unit~~ judges that the condition is satisfied, ~~to judge~~ whether ~~or not~~ data corresponding to the address generated by said address generator ~~generation unit~~ is stored in the cache;

a selector that selects ~~selection unit operable to select~~ a line within the cache ~~memory~~ in [[the]] a case where it is judged that the data is not stored;

an updater that performs ~~a write back unit operable to perform~~ a write back from the selected line when the selected line is valid and dirty; and

a registerer that registers ~~registration unit operable to register~~ the generated address as a tag, to the selected line, without transferring data from a memory to the selected line.

14. (Currently Amended) The cache memory system according to Claim 1,

wherein said manipulator ~~manipulation unit~~ includes:

a data judger that judges ~~judgment unit operable~~, in [[the]] a case where said judger ~~judgment unit~~ judges that the condition is satisfied, ~~to judge~~ whether ~~or not~~ data corresponding to the address generated by said address generator ~~generation unit~~ is stored in the cache;

a selector that selects a line, within the cache, in which data is stored ~~selection unit operable~~, in [[the]] a case where it is judged that the data is stored~~, to select a line, within the cache memory, in which the data is stored~~; and

an updater that performs ~~a write back unit operable to perform~~ a write back from the selected line when the selected line is valid and dirty.

15. (Currently Amended) The cache memory system according to Claim 1,

wherein said manipulator manipulates ~~manipulation unit~~ includes:

a data judger that ~~judgment unit operable~~, in the case where said judger ~~judgment unit~~ judges that the condition is satisfied, judges ~~to judge~~ whether ~~or not~~ data corresponding to the address generated by said address generator ~~generation unit~~ is stored in the cache;

a selector that selects a line within the cache in which data is stored ~~selection unit operable to select~~, in the case where it is judged that the data is stored~~, to select a line, within the cache memory, in which the data is stored~~;

an invalidator that invalidates ~~invalidation unit operable to invalidate~~ the selected line.

16. (Currently Amended) The cache memory system according to Claim 1,

wherein said manipulator ~~manipulation unit~~ includes:

a data judger that judges ~~judgment unit operable~~, in [[the]] a case where said judger ~~judgment unit~~ judges that the condition is satisfied, ~~to judge~~ whether ~~or not~~ data corresponding to the address generated by said address generator ~~generation unit~~ is stored in the cache;

a selector that selects a line, within the cache, in which data is stored ~~selection unit operable~~, in the case where it is judged that the data is stored~~, to select a line, within the cache memory, in which the data is stored~~; and

an updater that changes ~~a change unit operable to change~~ an access order of lines based on a selection by said selector ~~the selected line in order information indicating an order in which lines are accessed~~.

17. (Currently Amended) The cache memory system according to Claim 12,

wherein said condition generator generates ~~generation unit is operable to generate~~ a memory address as the condition, and

wherein said manipulator ~~manipulation unit~~ further includes

an adjuster that adjusts ~~adjustment unit operable~~, in [[the]] a case where the memory address generated by said condition generator ~~generation unit~~ indicates a point midway through a

line, to generate an address by adjusting so that one of a starting point of the line, a starting point of a next line, and a starting point of an immediately preceding line is indicated.

18. (Cancelled).

19. (New) A cache memory control method, comprising:

holding, by a condition generation information holder, information for generating a new condition, the information being obtained from a processor;

holding, by a command holder, a manipulation command obtained from the processor;

holding, by a condition holder, a condition relating to a state of the processor;

judging, by a judger, whether a current state of the processor satisfies the condition held by the condition holder;

generating, by an address generator, an address to be manipulated; and

manipulating, by a manipulator, a cache according to the manipulation command held by the command holder using the address generated by the address generator, when it is judged by the judger that the condition is satisfied; and

generating, by a condition generator, a new condition using one of the current state of the processor and the condition held by the condition holder, and the information for generating the new condition held by the condition generation information holder.